# System Integration at ASML: Linking Technical Content, Test Configurations, Timing… and People!

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# Introduction ASML

# System Integration at ASML

# System Integration pillars

- Technical content
- Test configurations
- Timing
- … and people!

# Lithography enables affordable connected electronics, improving quality of life and sustainability



**$1,469 B Electronic Applications in 2012**
$1,423 B in 2011, $1,343 B in 2010

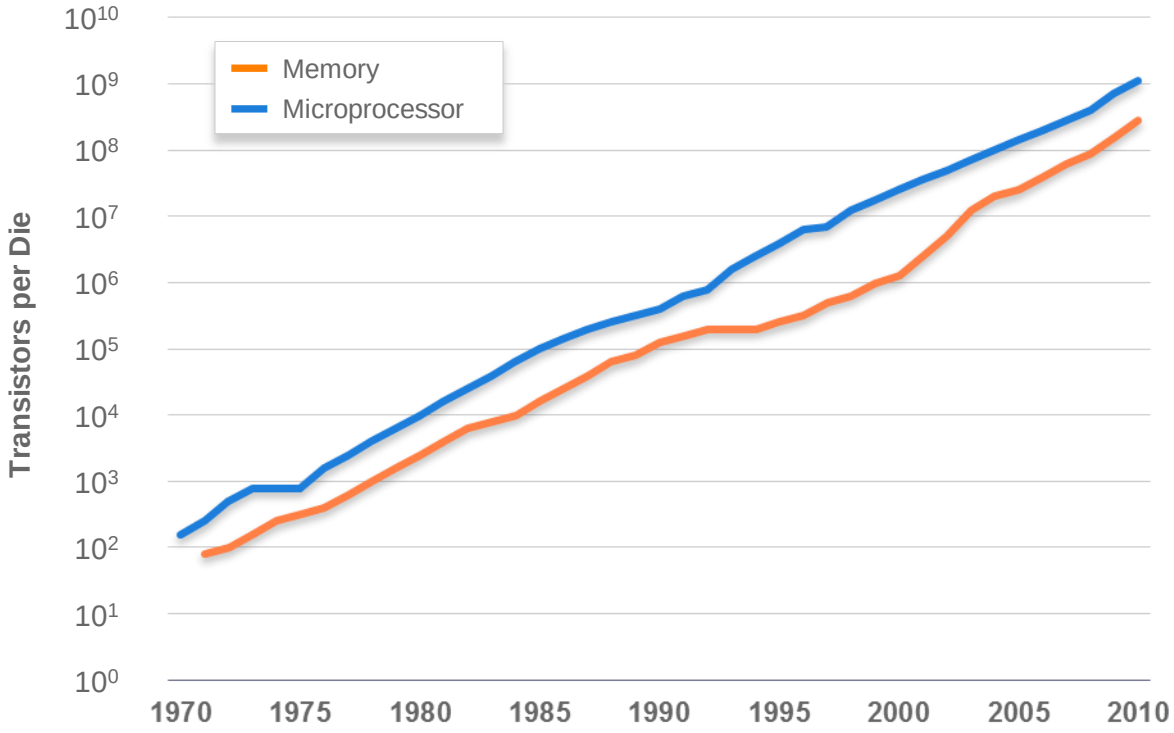
**$297.6 B Semiconductor Chips in 2012**
$306.8 B in 2011,
$301.5 B in 2010

**$ 6.5 B Semiconductor Litho market in 2012**
$8.2 B in 2011,
$6.4 B in 2010

Source: Gartner Q4/12 and ASML

# Moore’s Law holds steady for more than 40 years





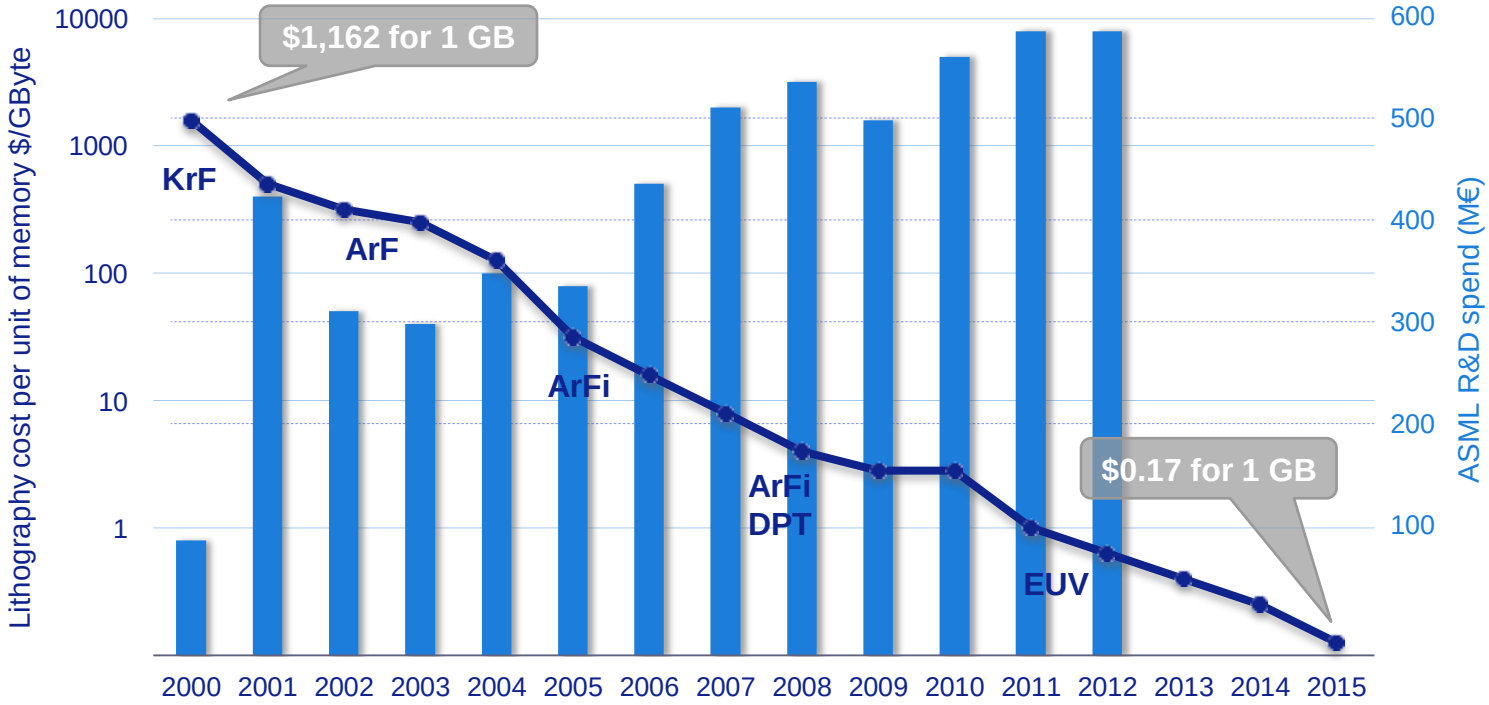

- Double the computing power per chip
- At equivalent power consumption
- For half the price
- Every 1.5 to 2 years

This graphic of Moore’s law shows how his prediction of transistor shrink has been realized over 40 years.

Source: Intel

# The economic benefit of shrink

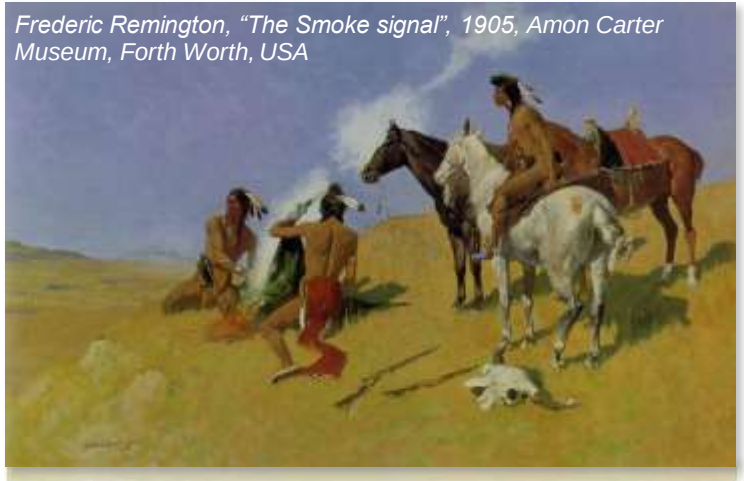
## At increasing R&D investments




Source: Gartner. High quality Flash

# Communication became ~ $10^{13}$ more energy efficient

## Enabled by scaling of semiconductors




**5 MJ/b**

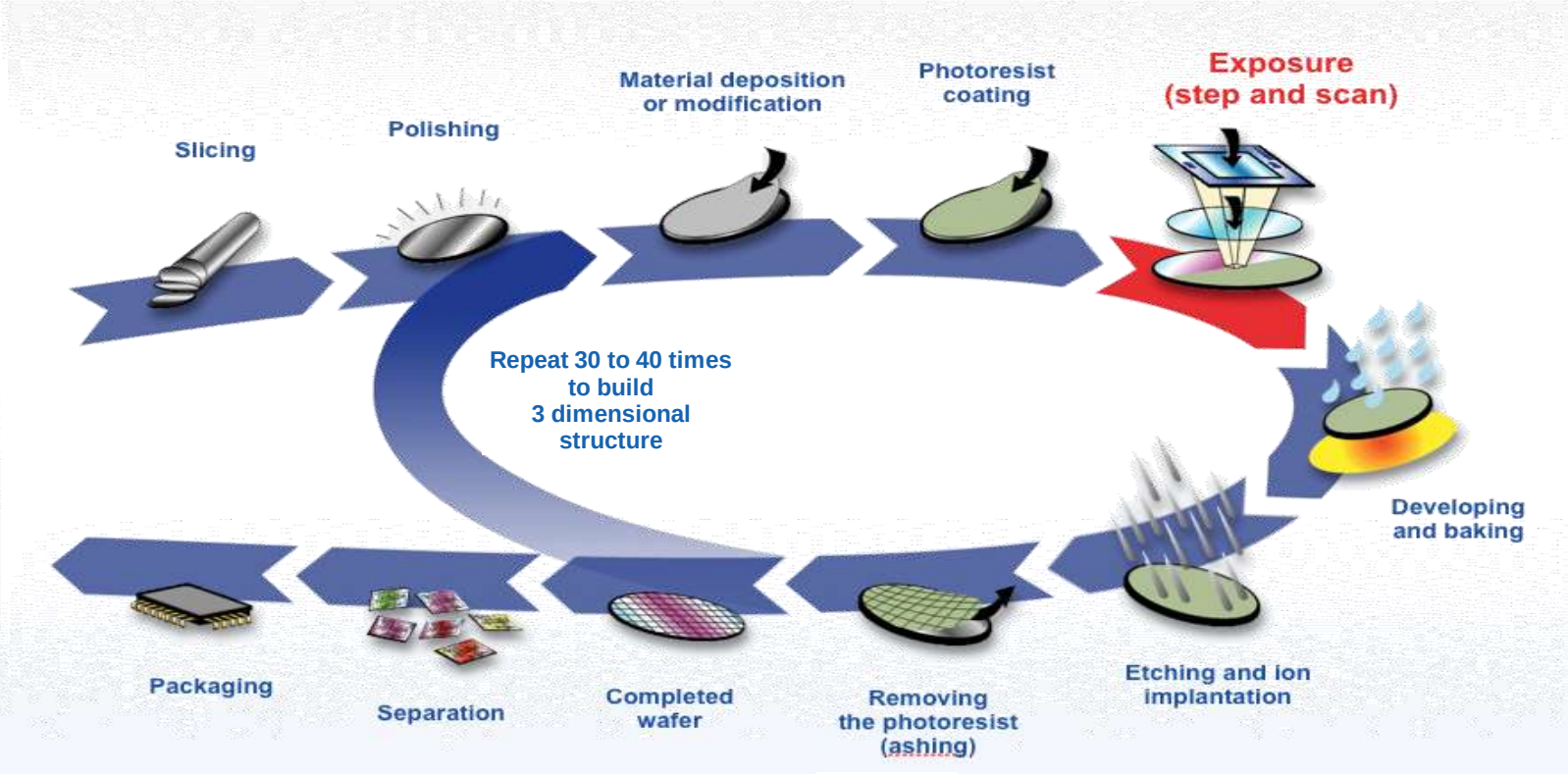
20 wood sticks of 2 cm diameter and 50 cm long equals ~3 dm³ Message size 10 characters or 10 ~15 MJ/dm³ energy from burning wood we use 45 MJ/message or 5 MJ/b

**1 µJ/b**

High Speed Downlink Packet Access, HSDPA speed 3.65 Mb/s using 5.5 W resulting in ~1µJ/b (Siemens UR5 router)

# Where does ASML fit in?

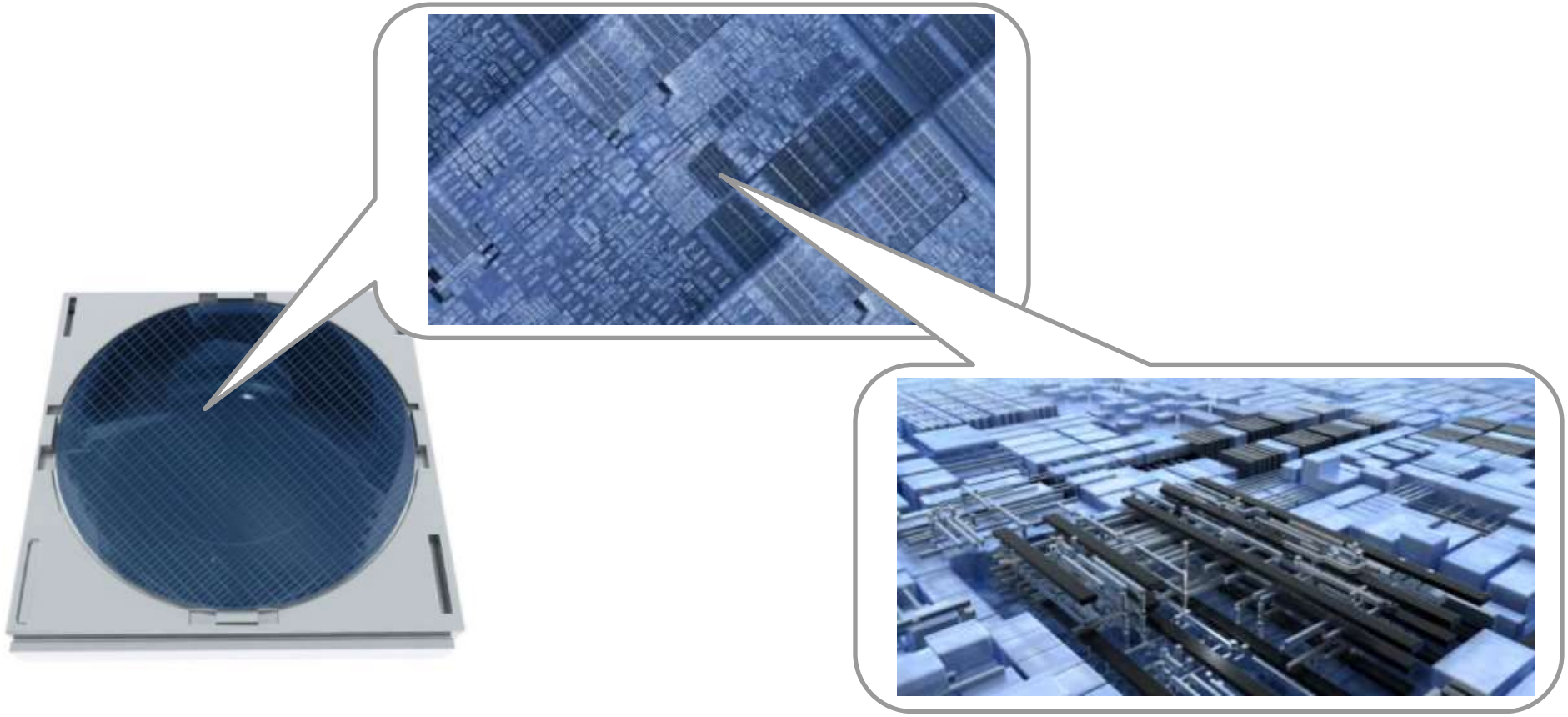
## Lithography is at the heart of chip manufacturing



# Zoom into a chip: this is nanometer accuracy

## Structures need to be aligned both horizontally and vertically

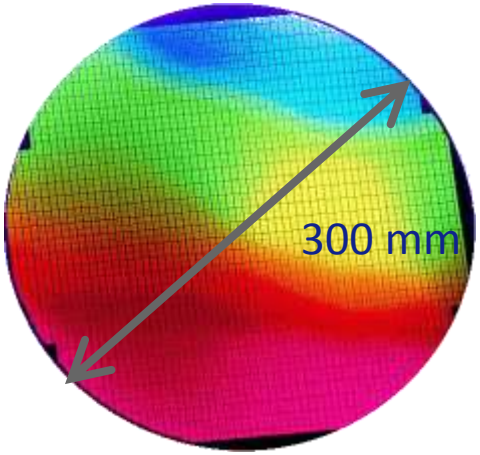




# Placement of these chip features is critical!

Equivalent: Print The Netherlands in 15 seconds!

**300 mm wafer**




**X1 million**

**The Netherlands**

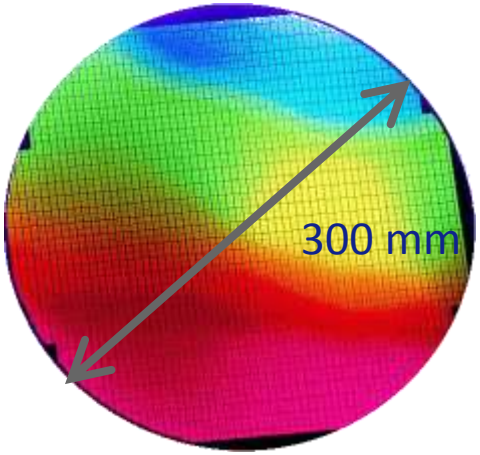

| | |
|---|---|
| Length of a field/chip | ~32 mm |
| Minimum feature size | ~20 nm |
| Positional accuracy | ~5 nm |

# Placement of these chip features is critical!



Equivalent: Print **South of Norway** in 15 seconds!

**300 mm wafer**



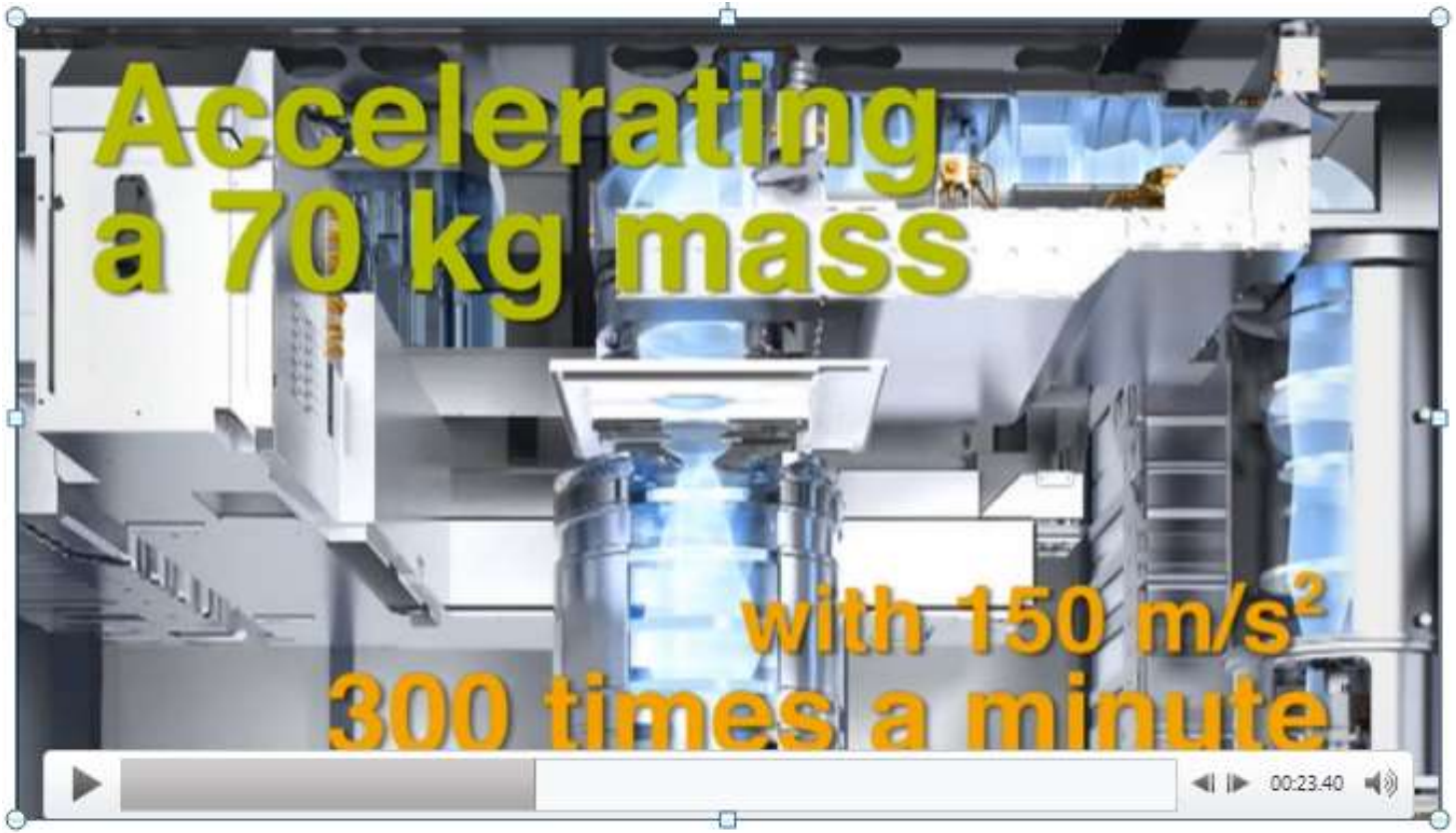

**X1 million**


| | | | |
|---|---|---|---|
| Length of a field/chip | ~32 mm | Corresponds to | ~32 km (KB-Drammen) |
| Minimum feature size | ~20 nm | | ~2 cm |
| Positional accuracy | ~5 nm | | ~5 mm |

# Photolithography – Main ASML system components

Although the basics are rather straightforward (“copy” pattern on reticle to wafer surface)…

# … the (conflicting) performance specs make it complex



# ASML: world's largest semiconductor equipment vendor

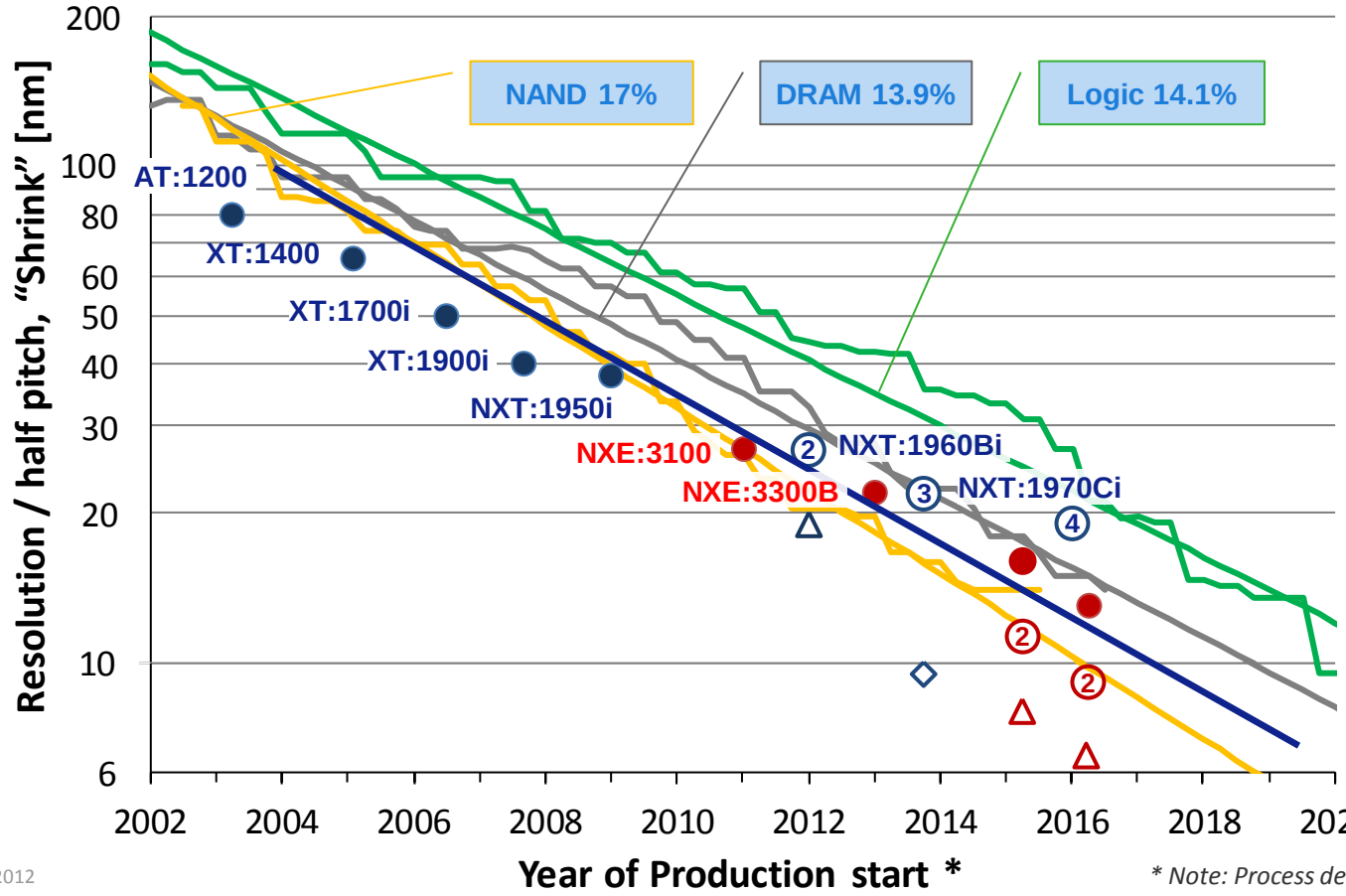

Over 55 sales and service offices located worldwide

Source: VLSI Research/ASML Q1 2013

# ASML headquarters in Veldhoven

# ASML products enable customer shrink roadmaps






*LE = Litho-Etch, n = number of iterations*

*SADP = Self Aligned Double Patterning*

*SAQP = Self Aligned Quadruple Patterning*

** Note: Process development 1.5 ~ 2 years in advance*

# Continuous lithography innovation: the shrink engine
## The smaller the lines, the bigger the systems…



In 30 years: From 1,200 nm to less than 20 nm resolution

**1984:**
**PAS 2000**
Resolution:
>1μm
Overlay: 250 nm

**1989:**
**PAS 5000**
Resolution:
<500 nm
overlay: 100 nm

**1990's:**
**PAS 5500 steppers/ scanners**
Resolution:
400 to 90 nm
overlay: 100 to 12 nm

**2000's:**
**TWINSCAN**
Resolution:
100 to 38 nm
overlay: 20 to 4 nm

**2010's:**
**NXE EUV systems**
Resolution:
32 to <20 nm
overlay: 2 nm

# ASML's leadership is the result of a talented workforce

Worldwide 8,625 employees as of Q1 2013

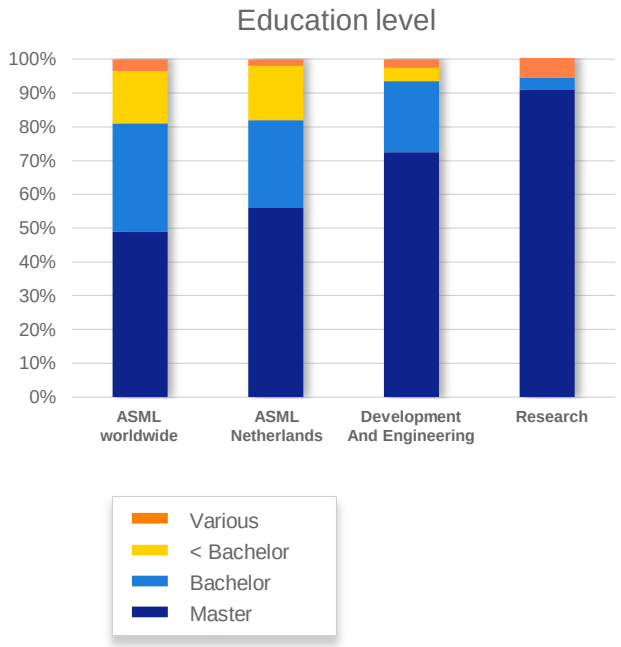
- R&D: >2,600 payroll + >1,300 contracted

49% of personnel has Master degree

- of which approximately 500 PhD's

Integrated knowledge network:

- another ~20,000 jobs at ~600 suppliers



Introduction ASML

**System Integration at ASML**

System Integration pillars

- Technical content
- Test configurations
- Timing
- … and people!

# System Integration at ASML



"The bringing together of subsystems into one system and ensuring that the subsystems function together and perform to specification"

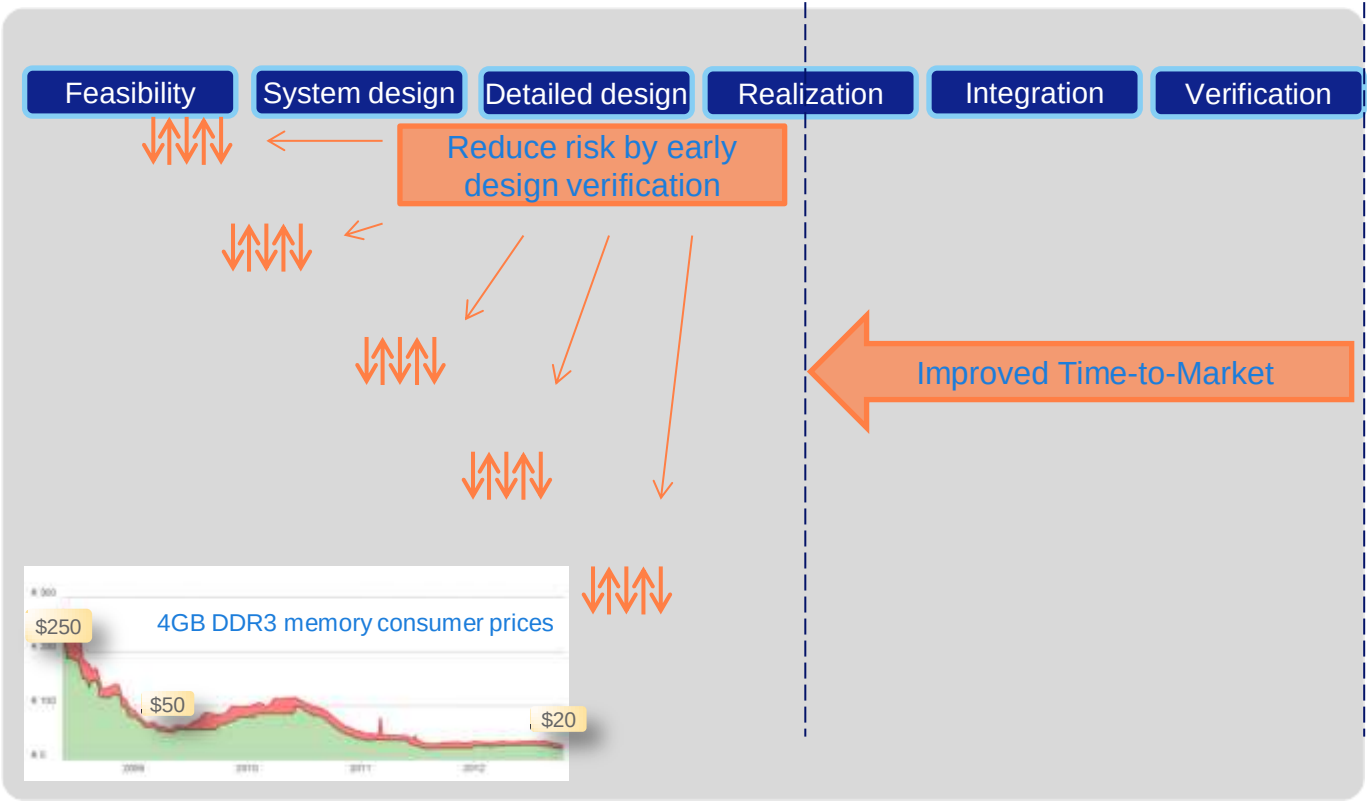
A typical ASML system integration project:

- Integrates ~2000 HW changes and ~1500 SW changes
- Takes ~1.5yr from first module available to first product shipment
- Involves ~20 delivering projects (~600 people)
- Consists of ~400 integration steps on system level
- Requires up to ~80M€ of testing resources
- Starts when not all requirements/designs are finished (next slide)

# Shorten Time-to-Market by concurrent engineering

## Early risk reduction during System Integration






Need short Time-to-Market:

- Customer chip ASP (declines fast in 1st year)
- ASML product ASP / ROI

Concurrent Engineering lets development phases overlap:

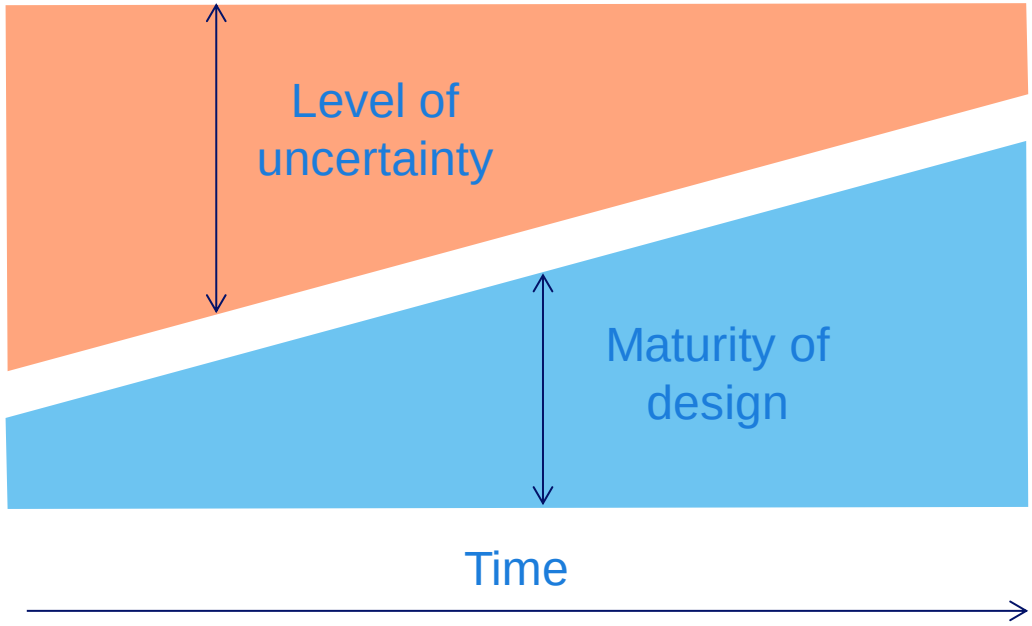
- Reduced total development time
- Early confrontation between design levels and disciplines
- Early requirements validation
- Early design verification as soon as possible

Known approach, but ASML applies this rather aggressively

# Concurrent Engineering & System Integration

## Reduction of design uncertainty over time



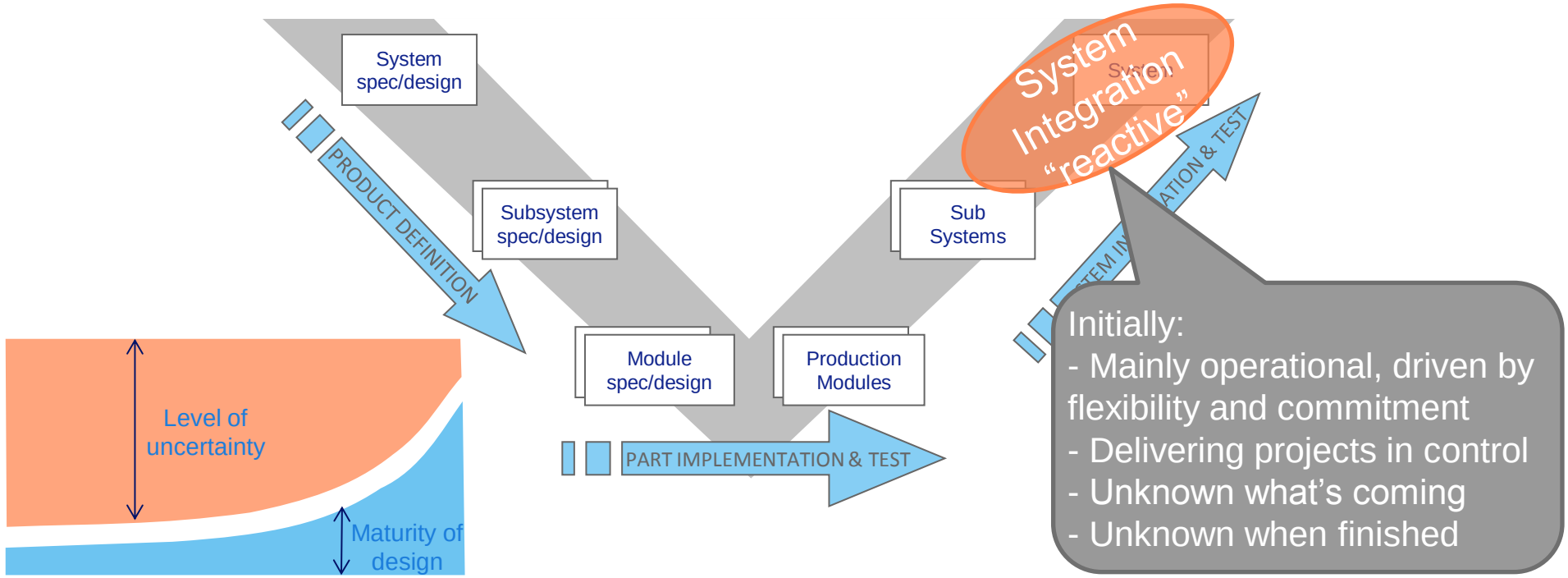



- Goal: steep slope!
- Start with key specs
- Risk management: focus on largest unknowns
  - What now, what later
  - Enable ordering of long lead items
- One thing is certain: things will change!

Maturity: combination of completeness and certainty w.r.t. specs

# System Integration and the (concurrent) V-model

0. Feasib. | 1. Reqs | 2. Design | 3. Proto | 4. Pilot | 5. Volume



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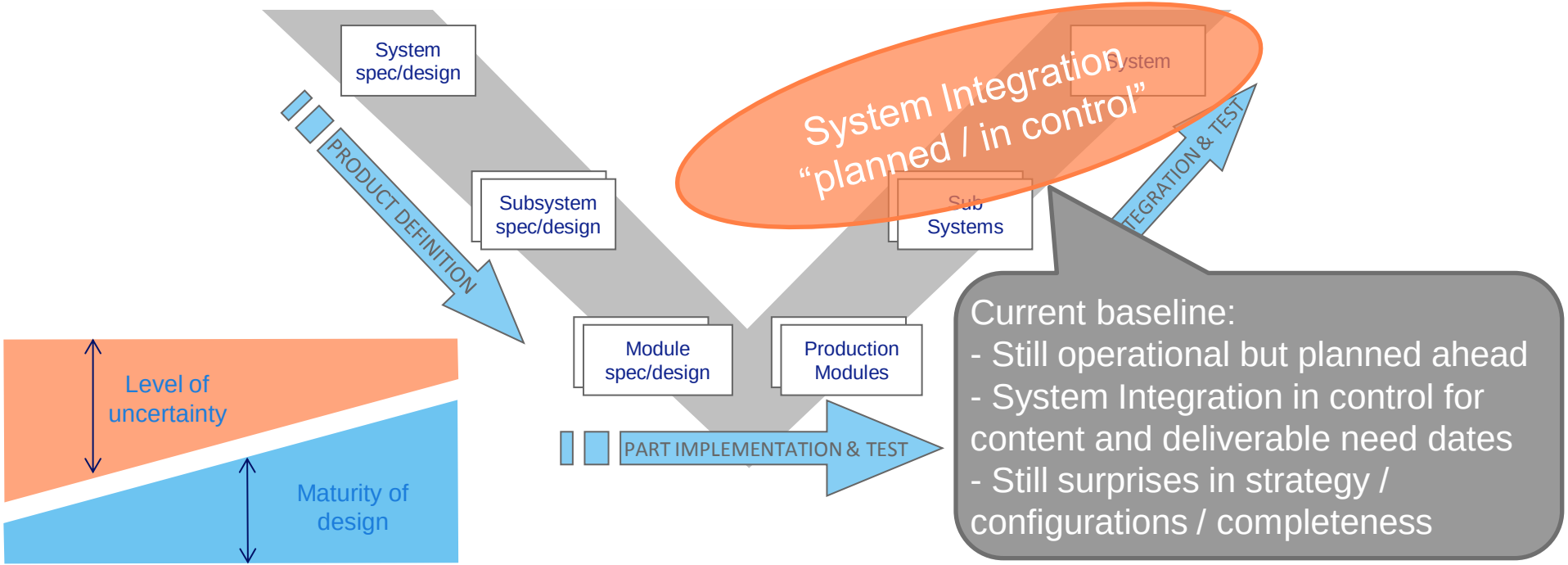

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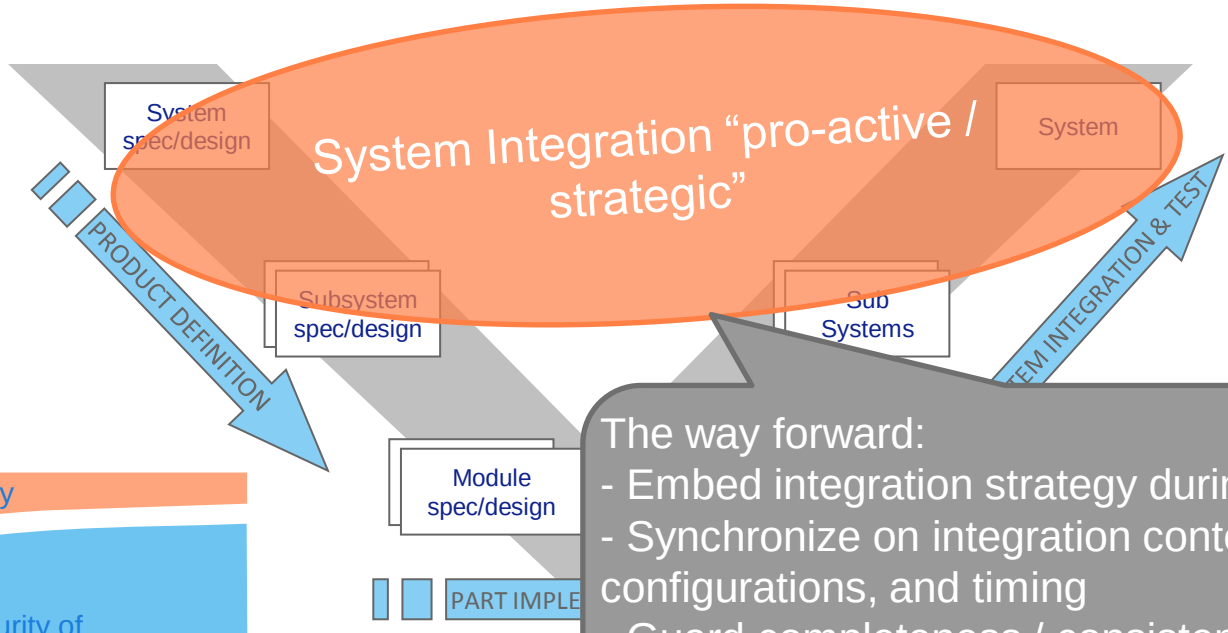
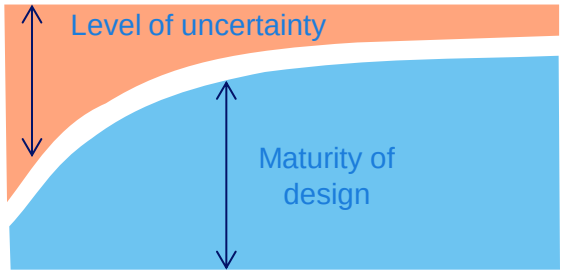



The way forward:
- Embed integration strategy during design phase
- Synchronize on integration content, test configurations, and timing
- Guard completeness / consistency / effective risk reduction all the time

Introduction ASML

System Integration at ASML

**System Integration pillars**

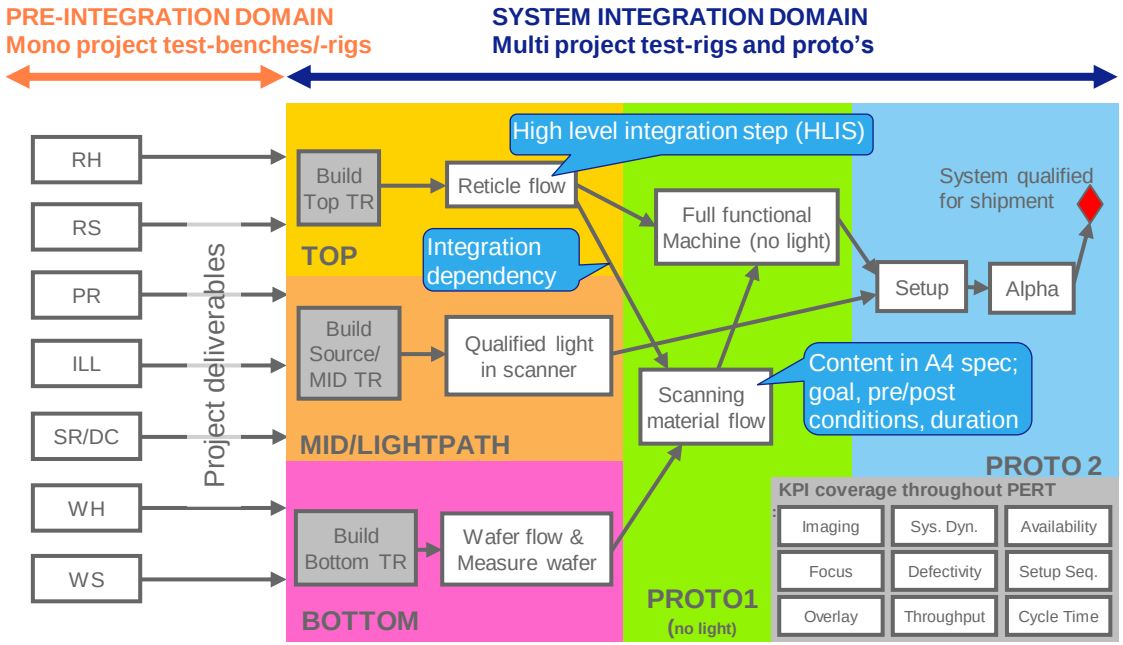
- Technical content
- Test configurations
- Timing
- … and people!

# System Integration pillars – TECHNICAL CONTENT

Integration strategy & content definition starts during design phase, based on:

- Breakdown of functional & performance requirements by Systems Engineering
- Masterplan by program management

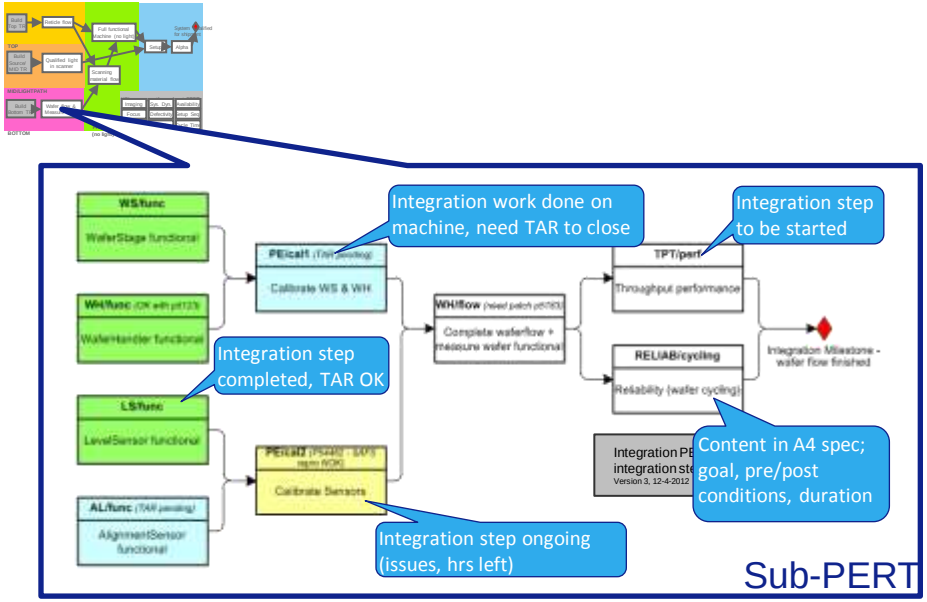
Integration “PERT” (logical overview of integration items)

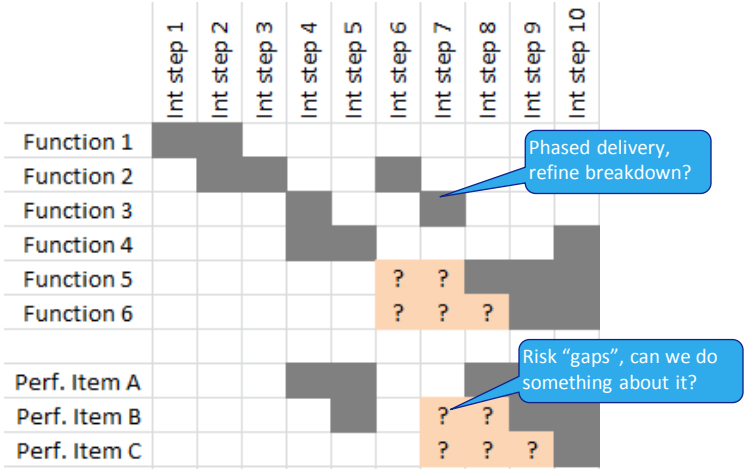


# System Integration pillars – TECHNICAL CONTENT

## Contents are refined via sub-PERTs:

- Assign integration steps to projects and track preparation/execution/closure status
- Guard completeness & pre/post conditions
- Analyze coverage of functional/performance breakdown incl. risk reduction effectivity



# System Integration pillars – TEST CONFIGURATIONS

Define, manage, and upgrade the required configuration baselines:

- In line with integration strategy, with intermediate configs to fill risk “gaps”
- Logical coupling to integration steps to derive correct deliverable need dates
  - E.g. project deliverable X is part of config baseline Y that is needed for integration step Z
    → need date of deliverable X is equal to the planned start date of int step Z (timing, 3rd pillar)
- Track actual machine configurations (plan upgrades to get known baselines)

Define config baseline in terms of deliverable HW/SW ID’s and settings

| Config baseline Y | Info | Machine 1 config | Machine 2 config | Machine 3 config | Machine 4 config |
|---|---|---|---|---|---|
| | | | | | |
| tem HW_253213 (2) | New machine part | OK | OK | 4 Item(s) | OK |
| HW-item HW_238701a , HW_238701b (2) | Interface connection extensions | HW_238701a HW_238701b | HW_238701a HW_238701b | HW_238701a HW_238701b | HW_238701a HW_238701b |
| HW-item HW_23849 (2) | Common support bracket | OK | OK | OK | OK |
| HW-item HW_21347 (1) | Dynamic performance improvement solution | 0 Item(s) | OK | 0 Item(s) | OK |
| SW-item SW_19a (>=1312) | Updated SW driver | wk311 | OK | OK | OK |
| SW-item SW_20b (>=1313) | Improved calibration test | wk311 | wk312 | OK | OK |
| Setting 1 (TYPE_B) | Setting for new machine part | OK | TYPE_A | OK | OK |
| Setting 2 (>120) | Setting for new calibration | OK | 100 | OK | OK |

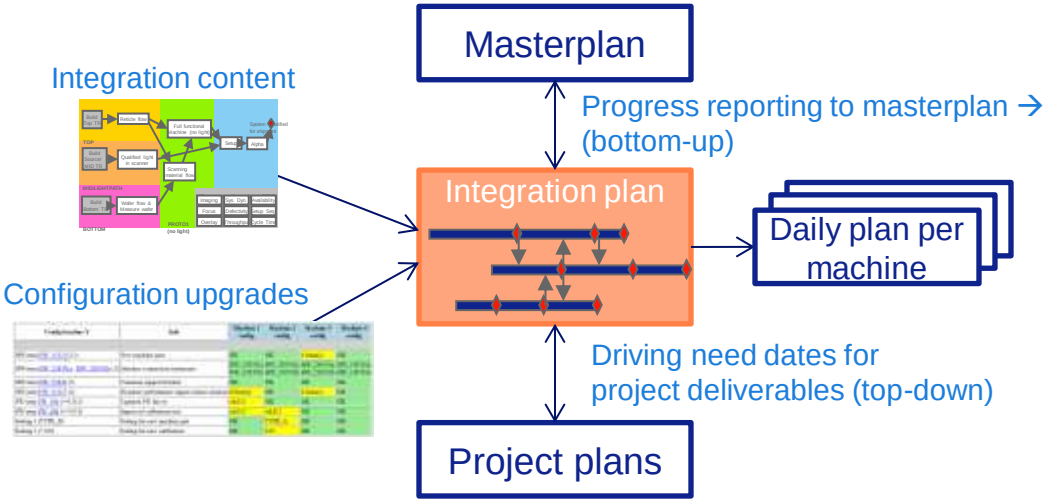
Machine 4 has correct configuration baseline to execute this int step

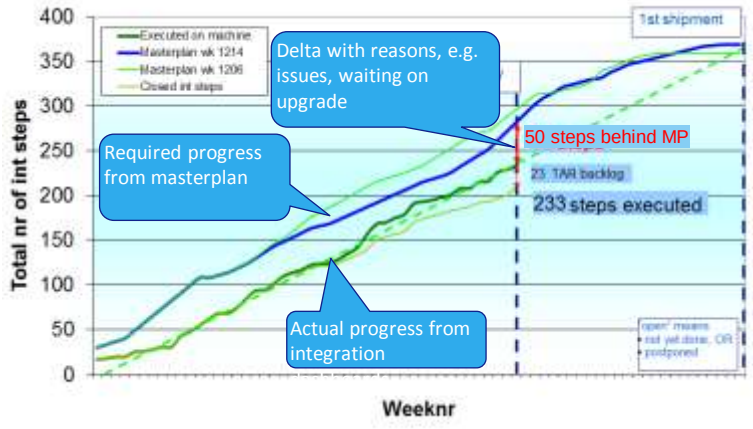
Other machines require upgrades to bring them to the same baseline

# System Integration pillars – TIMING

Integration plan combines inputs and manages allocation, timing, need dates:

- Based on integration step content and configuration upgrades (other pillars)
- Bridge between overall plan (weeks) to daily plan per machine (days/hours)
- Link integration plan activities to project deliverable plans (need dates)
- Consistent progress reporting towards masterplan



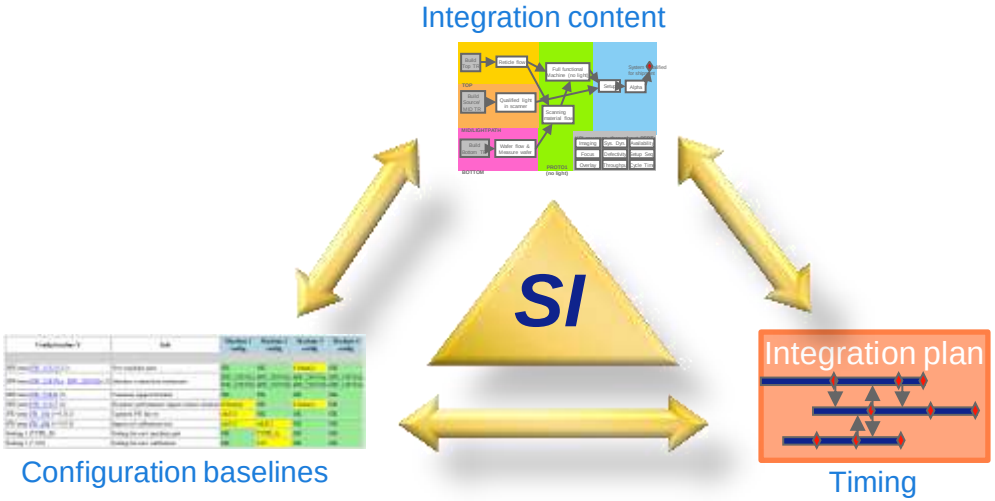



# The challenge of combining three SI pillars…



Get and keep the “SI golden triangle” of content/configurations/timing aligned

- A change in one of the pillars will influence the others (need flexibility to adapt)
- Things will change e.g. based on integration plan execution feedback/issues



# The challenge of combining three SI pillars…

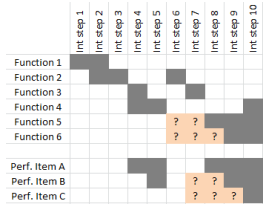
## … and the fourth "pillar" → PEOPLE!



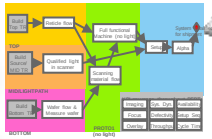
Get and keep things clear to the many stakeholders (100+) around SI…

- Embed this System Integration process in a learning organization

**SE/projects** (integration/risk coverage)

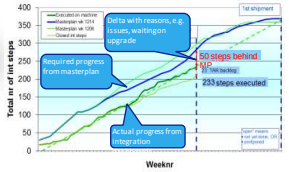



Integration content



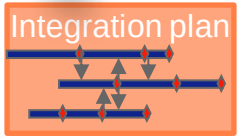
**Other programs**
(cross-deliverables)

**Program Management**
(progress reporting w.r.t. masterplan)




**SI**

Configuration baselines




Timing

**All ASML sectors**
(change management processes)

**Projects** (HW/SW deliverable definition & planning)

**Factory & support**
(final product baseline and procedures for volume production)

ASML

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System Integration is primarily about integrating people, the actual system will then follow by itself...